IN THE CLAIMS

Please amend the claims as shown in the following detailed claim listing. The detailed claim listing is intended to reflect the amendment of pending claims 1, 10, 15, and 17. The specific amendments to individual claims are detailed in the following detailed claim listing.

---

1. (Currently Amended) A method of preventing live-lock in a multiprocessor system, the method comprising:

identifying a first bus transaction ~~to~~ that attempts to modify a shared resource;

setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending; and

retrying each subsequent nonmodifying bus transaction for the shared resource until the status bit is cleared.

2. (Original) The method of claim 1 further comprising clearing the status bit when the first bus transaction completes.

A2

3. (Original) The method of claim 1 further comprising clearing the status bit randomly.

4. (Original) The method of claim 1 further comprising clearing the status bit at periodic intervals.

5. (Original) The method of claim 4 wherein the periodical intervals are longer than a length of time for a bus transaction to complete.

6. (Original) The method of claim 1 further comprising clearing the status bit using a pseudo-random method.

7. (Original) A method of preventing live-lock in a multiprocessor system, the method comprising:

issuing a first bus transaction that attempts to modify a cache line;

setting a status bit to indicate that a bus transaction attempting to modify the cache line is pending;

issuing a second bus transaction to read the cache line;

retrying the second bus transaction if the status bit is set;

reissuing the first bus transaction that attempts to modify the cache line; and

granting the cache line for the reissued first bus transaction if the status bit is set for the cache line.

8. (Original) The method of claim 7 further comprising clearing the status bit when the reissued first bus transaction complete.

A2

9. (Original) The method of claim 7 further comprising clearing the status bit pseudo-randomly.

10. (Currently Amended) A multiprocessor computer system comprising:

a plurality of processors;

a resource shared by the plurality of processors;

at least one system bus interconnecting the shared resource and the plurality of processors;

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on the at least one system bus by one of the processors; and

a status indicator associated with each one of the plurality of buffers, the status indicator ~~being set~~ to indicate when a first one of the processors initiates a bus transaction attempting to modify the shared resource and the bus transaction is retried.

11. (Original) The multiprocessor computer system of claim 10 wherein four processors are coupled to each one of the system buses.

12. (Original) The multiprocessor computer system of claim 10 wherein the at least one system bus comprises two processor buses.

13. (Original) The multiprocessor computer system of claim 10 having four processors coupled to each one of the two processor buses.

14. (Original) The multiprocessor computer system of claim 13 further comprising an input/output bus.

15. (Currently Amended) A multiple bus, multiprocessor computer system comprising:

a plurality of processors;

a plurality of data cache memories;

a system memory shared by the plurality of processors;

at least two buses interconnecting the system memory with the plurality of data cache memories and the plurality of processors; and

a controller comprising:

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on one of the buses by one of the processors; and

a status indicator associated with each one of the plurality of buffers, the status indicator ~~being set~~ to indicate when a first one of the processors initiates a bus transaction attempting to modify the system memory and the bus transaction is retried.

16. (Original) The multiple bus, multiple processor system of claim 15 wherein each one of the at least two buses is coupled to four of the processors.

17. (Currently Amended) An integrated circuit comprising:

a bus interface to control a plurality of bus transactions;

a coherency module to maintain cache coherency for a plurality of cache lines; and

a buffer manager comprising,

a plurality of buffers, each one of the buffers to store information associated with one of the plurality of bus transactions received by the bus interface; and

a plurality of status indicators to indicate that one of the bus transactions attempting to modify one of the cache lines is retried, at least one of the status indicators associated with each one of the buffers.

A2

18. (Original) The integrated circuit of claim 17 wherein the buffer manager further comprises logic to determine a type of bus transaction occurring on a bus.

19. (Original) The integrated circuit of claim 17 wherein the buffer manager further comprises logic to determine if two of the bus transactions are contending for a same cache line.

20. (Original) The integrated circuit of claim 17 further comprising logic to reset all of the plurality of status indicators.

21. (Original) The integrated circuit of claim 17 comprising 64 buffers and 64 status indicators.